No claims have been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Original) An interposer substrate for a flip chip semiconductor device assembly, comprising:

a first surface, an opposing second surface, and a dielectric member having a plurality of recesses extending thereinto from the first surface;

each recess of the plurality sized to substantially receive a conductive bump of at least one semiconductor die therein and exposing at least a portion of a conductive element at a bottom thereof, the plurality of recesses sized so that a gap will be left surrounding at least a portion of a conductive bump in at least some of the plurality of recesses; and

at least one opening extending through the interposer substrate, the at least one opening being in communication with the gaps.

2. (Original) The interposer substrate of claim 1, wherein the at least one opening comprises a plurality of passages extending to the plurality of recesses.

3. (Original) The interposer substrate of claim 2, wherein the plurality of passages comprises one or more passages extending to each of at least some of the plurality of recesses.

4. (Original) The interposer substrate of claim 1, wherein the at least one opening comprises a plurality of openings, each extending to a bottom portion of one of the plurality of recesses.

5. (Original) The interposer substrate of claim 1, wherein the at least one opening is formed through the second surface of the interposer substrate.

6. (Original) The interposer substrate of claim 1, wherein the at least one opening comprises a channel formed in the first surface of the interposer substrate and extending from one portion of a periphery of the interposer substrate to at least an interior portion thereof.

7. (Previously presented) The interposer substrate of claim 6, wherein a sidewall of the channel extends beside at least some of the plurality of recesses and opens into the at least some of the plurality of recesses in the interposer substrate.

8. (Original) The interposer substrate of claim 6, wherein the channel comprises a channel opening provided at the periphery of the interposer substrate, the channel opening configured to receive a dielectric filler material in nonsolid form.

9. (Original) The interposer substrate of claim 1, wherein the plurality of recesses comprises a recess configuration which is substantially a mirror image of a bond pad configuration on an active surface of the at least one semiconductor die.

10. (Original) The interposer substrate of claim 9, wherein the recess configuration comprises at least one of a center row recess configuration, an I-shaped recess configuration, and a peripheral recess configuration.

11. (Original) The interposer substrate of claim 1, wherein the second surface of the interposer substrate includes conductive balls on at least some of the conductive elements to electrically interconnect to external circuitry.

12. (Original) The interposer substrate of claim 1, wherein the dielectric member comprises a flexible dielectric tape.

13. (Original) The interposer substrate of claim 1, wherein the dielectric member comprises at least one of a polymer material, BT resin, FR4 laminate, FR5 laminate and ceramic.

14. (Previously presented) A wafer scale interposer substrate member, comprising:

a wafer scale dielectric member including multiple unsingulated interposer substrates, each arranged and dimensioned to correspond with one of the plurality of semiconductor dice on the wafer to be superimposed on the wafer scale interposer substrate member, each of the interposer substrates having a first surface, a second surface, and a plurality of recesses extending thereinto from the first surface, each recess sized to substantially receive a conductive bump of a semiconductor die of plurality of semiconductor dice of the wafer and exposing at least a portion of a conductive element at a bottom thereof, the plurality of recesses sized so that a gap will be left adjacent a portion of a conductive bump in at least some of the plurality of recesses; and

each of the interposer substrates including at least one opening in the dielectric member in communication with at least some of the gaps.

15. (Original) The member of claim 14, wherein the at least one opening comprises a plurality of passages extending to the plurality of recesses.

16. (Original) The member of claim 15, wherein the plurality of passages comprises one or more passages extending to one of the plurality of recesses.

17. (Original) The member of claim 14, wherein the at least one opening comprises a plurality of openings in each of the interposer substrates, each of the plurality of openings extending to a bottom portion of one of the plurality of recesses.

18. (Original) The member of claim 14, wherein the at least one opening is formed in the second surface of each of the interposer substrates.

19. (Original) The member of claim 14, wherein the at least one opening comprises at least one channel formed in the first surface of each of the interposer substrates and extends from a periphery of the wafer scale interposer substrate member to at least an interior portion thereof.

20. (Previously presented) The member of claim 19, wherein a sidewall of the at least one channel extends beside at least some of the plurality of recesses and opens into the at least some of the plurality of recesses.

21. (Original) The member of claim 19, wherein the at least one channel comprises at least one channel opening provided at a periphery of the wafer scale interposer substrate member, the at least one channel opening configured to receive a dielectric filler material in nonsolid form.

22. (Previously presented) The member of claim 14, wherein the plurality of recesses in each of the interposer substrates comprises a recess configuration which is substantially a mirror image of a bond pad configuration on an active surface of each of the plurality of semiconductor dice of the wafer.

23. (Original) The member of claim 22, wherein the recess configuration comprises at least one of a center row recess configuration, an I-shaped recess configuration, and a peripheral recess configuration.

24. (Original) The member of claim 14, wherein the second surfaces of the interposer substrates include conductive pads with conductive balls attached thereto.

25. (Original) The member of claim 14, wherein the dielectric member comprises a flexible dielectric tape.

26. (Original) The member of claim 14, wherein the dielectric member comprises at least one of a polymer material, BT resin, FR4 laminate, FR5 laminate and ceramic.